	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	L1	15908	SOI or "SOI" or silicon-on-insulat$4 or (silicon adj on adj insulat$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 17:07			0
2	BRS	L2	4163	implant$8 near15 (nitrogen or N2 or "N2" or "N.sub.2")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 18:58			0
3	BRS	L3	27666	implant$8 near8 (silicon or "Si" or Si)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 18:59			0
4	BRS	L4	325	1 and 2 and 3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 17:09			0
5	BRS	L5	2312	implant$8 near2 (nitrogen or N2 or "N2" or "N.sub.2")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 17:09			0
6	BRS	L6	11676	implant$8 near2 (silicon or "Si" or Si)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 17:10			0
7	BRS	L7	155	1 and 5 and 6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 17:10			0

4786608
5918151
5852346
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	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
8	BRS	L8	17	1 same 5 same 6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 19:01			0
9	BRS	L9	1543	implant$8 with (nitrogen or N2 or "N2" or "N.sub.2") with (silicon or "Si" or Si)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 18:59			0
10	BRS	L10	217	1 and 9	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 18:59			0
11	BRS	L11	7643	implant$8 near8 ((silicon or "Si" or Si) near2 (ion$1 or atom$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 19:03			0
12	BRS	L12	9	1 same 5 same 11	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 19:03			0
13	BRS	L13	4288	implant$8 near8 ((silicon or "Si" or Si) adj2 (ion$1 or atom$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 19:03			0
14	BRS	L14	0	1 same 5 same 13	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 19:04			0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
15	BRS	L15	50	1 and 5 and 13	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/26 19:04			0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	L1	7643	implant$8 near8 ((silicon or "Si" or Si) near2 (ion$1 or atom$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/27 16:13			0
2	BRS	L2	15908	SOI or "SOI" or silicon-on-insulat$4 or (silicon adj on adj insulat$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/27 16:14			0
3	BRS	L3	4163	implant$8 near15 (nitrogen or N2 or "N2" or "N.sub.2")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/27 16:14			0
4	BRS	L4	2312	implant$8 near2 (nitrogen or N2 or "N2" or "N.sub.2")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/27 16:14			0
5	BRS	L5	11676	implant$8 near2 (silicon or "Si" or Si)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/27 16:15			0
6	BRS	L6	155	2 and 4 and 5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/27 16:15			0
7	BRS	L7	17	2 same 4 same 5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/27 16:16			0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
8	BRS	L8	151	1 and 2 and 3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/27 16:17			0
9	BRS	L9	16	1 same 2 same 3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/27 16:24			0
10	BRS	L10	10	1 with 2 with 3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/11/27 16:19			0

US-PAT-NO: 4786608

DOCUMENT-IDENTIFIER: US 4786608 A

TITLE: Technique for forming electric field shielding layer in oxygen-implanted silicon substrate

---------- KWIC ---------

It should be noted that although, in the foregoing description of a preferred embodiment of the invention, **silicon ions are employed as the implant** species for forming the amorphous layer, other species of ions may be employed as the amorphizing implant formed near the interface of the buried oxide layer 13 and the **silicon-on-insulator** layer 14. For example, moderate doses of oxygen ions, e.g. on the order of 1.times.10.sup.16 O.sup.+ cm.sup.-2 (second oxygen implant), may be used. In addition, noble gas species, carbon, **nitrogen, or certain conventionally employed silicon dopants can be implanted** near the interface to form an amorphized layer. In each instance, as in the case of the silicon implant, the dosage is considerably lower than the initial oxygen implant and is carried out at room temperature for only several minutes, so that the characteristics of the amorphous region may be controlled with precision.

US-PAT-NO: 4509990

DOCUMENT-IDENTIFIER: US 4509990 A

TITLE: Solid phase epitaxy and regrowth process with controlled defect density profiling for heteroepitaxial semiconductor on insulator composite substrates

---------- KWIC ---------

By effectively precluding the use of high temperature annealing, a second problem was immediately realized. The crystalline quality of the silicon layer, as epitaxially deposited, was of insufficient quality to permit the fabrication of active devices therein. A process known as solid phase epitaxy (SPE) has been recently reported. See, S. S. Lau et al, "Improvement of Crystalline Quality of Epitaxial **Si Layers by Ion Implantation** Techniques", Applied Physics Letters, Vol. 34, No. 1, pp. 76-78, Jan. 1, 1979. The SPE process provides a low temperature subprocess for improving the crystallinity of the silicon epitaxial layer of a silicon-on-sapphire composite substrate.
The SPE process involves the high energy **implantation (typically at 250 keV to 600 keV) of an ion species, such as silicon,** into the silicon epitaxial layer at a sufficient dose to create a substantially amorphous silicon layer lying adjacent the silicon/sapphire interface while leaving a substantially crystalline layer at the surface of the original epitaxial layer. The thickness of the silicon epitaxial layer is substantially that intended for the completed **silicon-on-insulator** composite substrate (typically 4000 .ANG. or greater). The ion species is implanted through the

majority of the epitaxial
layer so that the maximum disruption of the silicon crystal lattice is near,
but not across, the silicon/sapphire interface to ensure that the amorphous
region is adjacent the sapphire substrate. Throughout the ion **implantation,
the sapphire substrate is maintained at a very low temperature, reported as
approximately that of liquid nitrogen** (77.degree. K.). A single step low
temperature (between 500.degree.-575.degree. C.) annealing of the composite
substrate is then performed to convert the amorphous silicon layer into
crystalline silicon. During this regrowth, the remaining crystalline surface
portion of the silicon layer effectively acts as a nucleation seed so that the
regrown portion of the silicon epitaxial layer has a common crystallographic
orientation and is substantially free of crystalline defects.

US-PAT-NO: 6352909

DOCUMENT-IDENTIFIER: US 6352909 B1

TITLE: Process for lift-off of a layer from a substrate

---------- KWIC ---------

Process for lift-off of a thin layer from a crystalline substrate, preferably
the layer from a silicon wafer to further form a **silicon-on-insulator (SOI)**
sandwich structure, wherein a separative interlayer comprises a thin
quasi-continuous gaseous layer and said interlayer is obtained by gettering a
monatomic hydrogen into a preformed buried defect-rich layer preferably
obtained by implantation. The monatomic hydrogen is preferably inserted into
the substrate by electrolytic means.

The present invention generally relates to processes for fabricating
silicon-on-insulator wafers, and more particularly, to a technology for
thinning of a semiconductor substrate by separating a layer from an initial
substrate with a hydrogen interlayer.

In previous art, a process for lift-off of a thin layer from a substrate has
been described by Gmitter at al. [1]. This process uses etching of sacrificial
layer. A disadvantage of the process is that the layer that can be lifted off
is limited to about 1 cm.sup.2 in area. Fabrication of **silicon-on-insulator**
wafers, however, currently requires lifting off layers with an area of 100 to
1000 cm.sup.2.

Yet another process for separating of semiconductor substrate is known due to

invention by Bruel [3]. In this process a gaseous interlayer is formed inside of semiconductor wafer by the sequence of process steps (1) implantation of hydrogen, (2) stiffening the surface that was implanted through to prevent blistering, and (3) transforming of the implanted hydrogen into quasi-continuous hydrogen layer. A disadvantage of the process is that a high implant dose is needed (10.sup.17 /cm.sup.2 for monatomic hydrogen or 5.times.10.sup.16 /cm.sup.2 for diatomic hydrogen). The total cost of the SOI-end-product wafer using this process is increased by the cost of the implantation.

Another improvement of Bruer s process is described in the invention by Henley at al. [5]. This process uses plasma immersion ion implantation instead of conventional implantation to insert hydrogen into silicon. A disadvantage of the process is that plasma immersion implantation results in an energy distribution of incident hydrogen over a wide energy range to about 50-80 keV. This results in a lo times increase of minimum implant dose needed for cleavage (i.e. 10.sup.18 cm.sup.2 instead of 10.sup.17 cm.sup.2). This high dose damages the layer to be lifted off, and the quality of the final SOI wafer is lower as compared to wafers obtained using Bruel's process. Another problem of plasma immersion is that the high dose implantation can result in severe damage to the wafer surface. This surface should be immediately attached (without any intermediate heat treatment to heal the surface) after implantation to a stiffener wafer. Prebonding of the damaged surface to another surface is not effective. Thus plasma immersion lowers the production yield of **silicon-on-insulator** wafers significantly.

The present invention relates to a method for lifting off of a thin layer from a crystalline substrate. The fractured layer may be further attached to another substrate thus forming, for example a **silicon-on-insulator (SOI**) wafer.

This invention reduces the ion implantation dose needed for the lift-off process. Said ion implant dose is decreased by more then an order of magnitude compared to conventional hydrogen processes. Furthermore, the disclosed process permits a thinner top silicon layer in the final **SOI** wafer with better thickness control then can be obtained with the conventional processes.

The embodiment which will now be described shows a method for the lift-off of a thin layer from a monocrystalline silicon substrate. The released layer maybe further transferred onto a second substrate that is the stiffener. This preferred embodiment involves trap-inducing **silicon ion implantation into the silicon** substrate followed by an electrolytic charging of the traps in the silicon substrate with hydrogen. The initial silicon substrate is schematically shown on FIG. 2A.

530 micrometer-thick monocrystalline silicon substrates with (100) crystallographic surface orientation are used. A 500 .ANG.-thick thermal oxide covers the surface of the silicon substrate. The trap inducing **implantation 2, FIG. 2B is performed with singly and positively charged silicon ions** at 180 keV with a dose of 5.times.10.sup.14 cm.sup.-2. The implantation forms a implanted silicon depth concentration distribution with a maximum at a depth R.sub.p of approximately 0.5 micrometers. Maximum concentration of displaced atoms occurs at a depth of 1/2R.sub.p =0.25 micrometers. The wafer temperature is

maintained near room temperature during implantation. The wafer is preferably
kept at lowest possible temperature during implantation. It maximizes number
of traps for hydrogen created.

With heavy ion implants the buried amorphized layer begins not deeper than 0.1
micrometer even at high .about.300 keV energy. Layers thinner than about 0.1
micrometer can be lifted-off using heavy ion implants. For facilitating
lift-off of layers of less than 0.1 micrometer thickness heavy ions are
preferable. Medium mass ions allow layer up to 0.5-0.8 micrometers thickness
to be lifted-off. For the manufacture of **SOI** wafers in mainstream state of the
art CMOS ULSI with feature size of 0.18 micrometers, medium mass ions are
preferable for creating the amorphized region. The lightest ions (protons)
permit lift-off of layers up to 10 micrometers thick for 1.6 MeV protons
implanted at a dose of 10.sup.14 cm.sup.-2 and with the substrate at liquid
nitrogen temperature. Use of the lightest ions is preferable for fabricating
thick top layer **SOI** for applications such as MEMS, power transistors and p-i-n
diodes. An additional advantage of using the lightest ions is that blistering
phenomena is suppressed. Accordingly, thick layer can be lifted off without
using a stiffener wafer.

It is generally preferable that the ion implant specie used to form the trap
layer does not contaminate or dope silicon. From this consideration, the best
implants are silicon ions. However, implanting of electrically inactive
species like helium is also appropriate.

This preferred embodiment may be compared to separation using direct plasma
immersion ion implantation [5]. The comparison is given to show an advantage

of the inventive process over the process due to [5]. The process [5] requires
an implant dose of 10.sup.18 cm.sup.-2 or larger. The process due to present
invention delivers hydrogen predominantly into thin, buried trap layer.
Therefore, lower (.about.10.sup.17 cm.sup.-2) amount of hydrogen is needed for
the separation. In the present invention, low energy plasma can be used,
because the hydrogen is delivered to a predetermined depth by a diffusion
process, and not by implantation action of plasma alone. Accordingly, the top
silicon layer is not deeply damaged allowing fabricating high quality **SOI**
wafers.

18. A method for making a **silicon-on-insulator** wafer, comprising:

DERWENT-ACC-NO: 1996-458049
DERWENT-WEEK: 199646

TITLE: **SOI** structure formation method used in electronic component such as
semiconductor device - involves forming ion implantation layer by making ion
implantation of O_2, N_2 into inside of silicon substrate, as stopper layer
during polishing

PATENT-ASSIGNEE: SONY CORP[SONY]

PRIORITY-DATA: 1991JP-0313700 (October 31, 1991)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 06097398 A	April 8, 1994	N/A	006	H01L 027/12

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 06097398A	N/A	1991JP-0313700	October 31, 1991

INT-CL (IPC): H01L021/265; H01L021/304 ; H01L021/76 ; H01L021/84 ;
H01L027/12

ABSTRACTED-PUB-NO: JP 06097398A
BASIC-ABSTRACT: The method involves forming an insulated layer (2) such as SiO2
layer on the surface of one side and a silicon portion (10) on the surface of
other side of a silicon substrate (1). A second substrate (4) is combined with
the insulated layer of the silicon substrate.

An ion implantation layer (5) is formed by making ion **implantation of O2, N2**
into the inside of the silicon substrate, as stopper layer during polishing.

ADVANTAGE - Prevents size dependance of **SOI** pattern, thereby enabling to obtain homogenous **SOI** layer. Avoids influence of warpage of substrate wafer, which originates in alignment process.

CHOSEN-DRAWING: Dwg.1/2

TITLE-TERMS:
SOI STRUCTURE FORMATION METHOD ELECTRONIC COMPONENT SEMICONDUCTOR DEVICE
FORMING ION IMPLANT LAYER ION **IMPLANT N SILICON** SUBSTRATE STOPPER LAYER POLISH

DERWENT-CLASS: U11

EPI-CODES: U11-C08A6;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1996-386021

US-PAT-NO: 5395771

DOCUMENT-IDENTIFIER: US 5395771 A

TITLE: Graded implantation of oxygen and/or nitrogen constituents to define buried isolation region in semiconductor devices

---------- KWIC ---------

The invention is generally directed to semiconductor fabrication. The invention is more specifically directed to the formation of a buried isolation region using **implantation of oxygen, nitrogen** or other insulation-forming particles into a single crystal semiconductor substrate.

Traditional isolation techniques create a homogenous high doping concentration of insulative molecules within the substrate. In a silicon (Si) substrate for example, a concentration of approximately 2.times.10.sup.18 atoms/cm.sup.2 of oxygen is provided uniformly across a buried insulator region of one-half micron (0.5 .mu.m) or greater thickness. High energy implantation is used to introduce oxygen atoms into a subsurface region of a semiconductor substrate. When the substrate is monocrystalline **silicon, the silicon atoms combine with the implanted** 0 atoms to produce SiO.sub.2.

D. Hill et al., J. Appl. Phys., 63(10) 15 May 1988, 4933 "The reduction of dislocations in O implanted **SOI** by seq. ion impl."

S. N. Bunker et al., Mat. Res. Soc. Symp. Proc., vol. 93 p. 125 "Formation of **SOI** Structures by multiple oxygen implantations".